UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/066,833	02/04/2002	Tomasz Konrad Skrzeszewski	NL 010065	4833

7590 08/18/2005

U.S. Philips Corporation
345 SCARBOROUGH ROAD
BRIARCLIFF MANOR, NY 10510

EXAMINER	
MEONSKE, TONIA L	
ART UNIT	**PAPER NUMBER**
2183	

DATE MAILED: 08/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/066,833	SKRZESZEWSKI ET AL.	
	Examiner	Art Unit	
	Tonia L. Meonske	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 June 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 February 2005* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference character(s) that are not mentioned in the description: Figure 1 and 3 elements 144, 162, and 300. Corrected drawing sheets in compliance with 37 CFR 1.121(d), or amendment to the specification to add the reference character(s) in the description in compliance with 37 CFR 1.121(b) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

2. The disclosure is objected to because of the following informalities: There are no headings to indicate sections in the specification. Headings are needed for the sections: Background of the Invention, Field of the Invention, Description of the Related Art, Brief Summary of the Invention, Brief Description of the Several Views of the Drawings, and Detailed Description of the Invention. For Applicant's convenience, the content of specification from the MPEP is included below. Appropriate corrections are required.

Content of Specification

(a) Title of the Invention: See 37 CFR 1.72(a) and MPEP § 606. The title of the invention should be placed at the top of the first page of the specification unless the title is provided in an application data sheet. The title of the invention should be brief but technically accurate and descriptive, preferably from two to seven words may not contain more than 500 characters.

(b) Cross-References to Related Applications: See 37 CFR 1.78 and MPEP § 201.11.

(c) Statement Regarding Federally Sponsored Research and Development: See MPEP § 310.

(d) Incorporation-By-Reference Of Material Submitted On a Compact Disc: The specification is required to include an incorporation-by-reference of electronic documents that are to become part of the permanent United States Patent and Trademark Office records in the file of a patent application. See 37 CFR 1.52(e) and MPEP § 608.05. Computer program listings (37 CFR 1.96(c)), "Sequence Listings" (37 CFR 1.821(c)), and tables having more than 50 pages of text were permitted as electronic documents on compact discs beginning on September 8, 2000.

Or alternatively, Reference to a "Microfiche Appendix": See MPEP § 608.05(a). "Microfiche Appendices" were accepted by the Office until March 1, 2001.

(e) Background of the Invention: See MPEP § 608.01(c). The specification should set forth the Background of the Invention in two parts:

(1) Field of the Invention: A statement of the field of art to which the invention pertains. This statement may include a paraphrasing of the applicable U.S. patent classification definitions of the subject matter of the claimed invention. This item may also be titled "Technical Field."

(2) Description of the Related Art including information disclosed under 37 CFR 1.97 and 37 CFR 1.98: A description of the related art known to the applicant and including, if applicable, references to specific related art and problems involved in the prior art which are solved by the applicant's invention. This item may also be titled "Background Art."

(f) Brief Summary of the Invention: See MPEP § 608.01(d). A brief summary or general statement of the invention as set forth in 37 CFR 1.73. The summary is separate and distinct from the abstract and is directed toward the invention rather than the disclosure as a whole. The summary may point out the advantages of the invention or how it solves problems previously existent in the prior art (and preferably indicated in the Background of the Invention). In chemical cases it should point out in general terms the utility of the invention. If possible, the

nature and gist of the invention or the inventive concept should be set forth. Objects of the invention should be treated briefly and only to the extent that they contribute to an understanding of the invention.

(g) Brief Description of the Several Views of the Drawing(s): See MPEP § 608.01(f). A reference to and brief description of the drawing(s) as set forth in 37 CFR 1.74.

(h) Detailed Description of the Invention: See MPEP § 608.01(g). A description of the preferred embodiment(s) of the invention as required in 37 CFR 1.71. The description should be as short and specific as is necessary to describe the invention adequately and accurately. Where elements or groups of elements, compounds, and processes, which are conventional and generally widely known in the field of the invention described and their exact nature or type is not necessary for an understanding and use of the invention by a person skilled in the art, they should not be described in detail. However, where particularly complicated subject matter is involved or where the elements, compounds, or processes may not be commonly or widely known in the field, the specification should refer to another patent or readily available publication which adequately describes the subject matter.

(i) Claim or Claims: See 37 CFR 1.75 and MPEP § 608.01(m). The claim or claims must commence on separate sheet or electronic page (37 CFR 1.52(b)(3)). Where a claim sets forth a plurality of elements or steps, each element or step of the claim should be separated by a line indentation. There may be plural indentations to further segregate subcombinations or related steps. See 37 CFR 1.75 and MPEP § 608.01(i)-(p).

(j) Abstract of the Disclosure: See MPEP § 608.01(f). A brief narrative of the disclosure as a whole in a single paragraph of 150 words or less commencing on a separate sheet following the claims. In an international application which has entered the national stage (37 CFR 1.491(b)), the applicant need not submit an abstract commencing on a separate sheet if an abstract was published with the international application under PCT Article 21. The abstract that appears on the cover page of the pamphlet published by the International Bureau (IB) of the World Intellectual Property Organization (WIPO) is the abstract that will be used by the USPTO. See MPEP § 1893.03(e).

(k) Sequence Listing, See 37 CFR 1.821-1.825 and MPEP §§ 2421-2431. The requirement for a sequence listing applies to all sequences disclosed in a given application, whether the sequences are claimed or not. See MPEP § 2421.02.

Claim Objections

3. Claims 7, 8, 9, 10, and 12 objected to because of the following informalities: In the claims there are reference numbers that refer to elements in the figures. These reference numbers have not effect on the scope of the claim as stated by 608.01(m) in the MPEP. If it is the applicants desire to have the claims limited by the drawings then the applicant should rewrite the claims stating what limitations should be applied without referring to the drawings. Appropriate correction is required. In this office action and all subsequent office actions, no weight will be given to reference numbers in the claims.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claim 4 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

6. Claim 4 recites the limitation "said insertion means" in lines 3 and 4. There is insufficient antecedent basis for this limitation in the claim. For the rest of this office action it is assumed that said insertion means refers to forcing an instruction into the pipeline of the processor from claim 1.

7. Claim 4 contains a reference to said instruction B that has been inserted into said first intermediate pipeline stage by said insertion means in lines 2-4 of the claim. Claim 4 is dependent on claim 1 and claim 1 contains an instruction A and an instruction B. Instruction A in claim 1 is inserted into the first intermediate pipeline stage and instruction B is not being inserted and is the instruction that resides in the second intermediate stage of the pipeline. For

the rest of this office action It is assumed that instruction B in claim 4 line 2 is meant to be instruction A and that it is a typo.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

9. Claims 1, 4, 5, 7, and 12 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Hammer et al., US Patent 5,901,309 (herein referred to as Hammer).

10. Referring to claim 1, Hammer has taught a method for manipulating an instruction flow in a pipeline of a processor, comprising the following steps:

a. detecting a stimulus leading to a disruption of progress of an instruction through a pipeline (abstract, Figure 4, column 2, lines 8-38, column 3, line 51-column 4, line 39, An interrupt is detected.);

b. on detecting said stimulus, causing multiple pipeline stages to become available by performing a pipeline flush, and forcing an instruction A required for responding to said stimulus by said processor directly into a first intermediate pipeline stage (abstract, Figure 4, column 2, lines 8-38, column 3, line 51-column 4, line 39, ISI(1) and ISI(2) are inserted into the pipeline to service the interrupt. Flushed instructions as a result of the inserted instructions are fetched again.), said intermediate stage becoming available as a result of said disruption (abstract, Figure 4, column 2, lines 8-38, column 3, line 51-column 4, line 39, The pipeline stages are available for the inserted interrupt service

instructions.), characterized in that said stimulus is detected from an instruction type of an instruction B residing in a second intermediate stage of the pipeline (abstract, Figure 4, column 2, lines 8-38, column 3, line 51-column 4, line 39, An interrupt type instruction is detected in the pipeline during instruction execution.).

11. Referring to claim 4, Hammer has taught a method according to claim 1, as described above, and characterized in that said instruction B is an interrupt call that has been inserted into said first intermediate pipeline stage by said insertion means (abstract, Figure 4, column 2, lines 8-38, column 3, line 51-column 4, line 39).

12. Referring to claim 5, Hammer has taught a method according to claim l, as described above, and characterized in that said instruction B is a programmable instruction causing a pipeline flush (column 3, line 51-column 4, line 62).

13. Referring to claim 7, Hammer has taught a system for manipulating an instruction flow, comprising:

a. a processing pipeline (figure 3, element 55);

b. detection means for detecting a stimulus leading to a disruption of the progress of an instruction through said pipeline (abstract, Figure 4, column 2, lines 8-38, column 3, line 51-column 4, line 39, An interrupt is detected.);

c. means for causing multiple pipeline stages to become available by performing a pipeline flush (abstract, Figure 4, column 2, lines 8-38, column 3, line 51-column 4, line 39, Interrupt service instructions are inserted into the pipeline, causing other instructions in the pipeline to be effectively flushed and fetched again.); and insertion means, responsive to said detection means, for forcing an instruction A directly into a first

intermediate pipeline stage (abstract, Figure 4, column 2, lines 8-38, column 3, line 51-column 4, line 39, ISI(1) and ISI(2) are inserted into the pipeline to service the interrupt. Flushed instructions as a result of the inserted instructions are fetched again.), said stage becoming available as a result of said disruption (abstract, Figure 4, column 2, lines 8-38, column 3, line 51-column 4, line 39, The pipeline stages are available for the inserted interrupt service instructions.), characterized in that said stimulus is detectable from an instruction type of an instruction B residing in a second intermediate stage of the pipeline (abstract, Figure 4, column 2, lines 8-38, column 3, line 51-column 4, line 39, An interrupt type instruction is detected in the pipeline during instruction execution.).

14. Referring to claim 12, Hammer has taught a system according to claim 7, as described above, and characterized in that the instruction A to be forced into a pipeline by said insertion means is stored in a data storage device (column 4, lines 7-20 and 29-39.).

Claim Rejections - 35 USC § 103

15. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

16. Claims 2, 3, and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hammer et al., US Patent 5,901,309 (herein referred to as Hammer) in view of Intel Architecture Software Developer's Manual, Volume 1: Basic Architecture, cited by the Examiner in the action mailed on August 8, 2004 (herein referred to as Intel).

17. Referring to claim 2, Hammer has taught a method according to claim 1, as described above. Hammer has not taught the method is characterized in that said instruction A causes the processor to store a processor status on a stack. However, Hammer has taught that once the processor has finished processing an interrupt, normal processing is resumed, see column 1, lines 18-22, column 2, lines 35-39. Hammer has omitted the details of resuming normal processing after an interrupt. However, in order for the processor to resume normal processing after the interrupt is serviced, the processor status must be saved upon an interrupt. Intel has taught interrupt instructions that cause the processor to store a processor status on a stack for the desirable purpose of quickly resuming execution of the interrupted instructions (Intel, page 4-15, lines 1-4 and page 4-16 lines 7-8. The contents of the EFLAGS, CS, and EIP registers are the processor status.). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have the instruction A of Hammer, cause the processor to store a processor status on a stack, as taught by Intel, for the desirable purpose of quickly resuming execution of the interrupted instructions.

18. Referring to claim 3, Hammer has taught a method according to claim 1, as described above. Hammer has not specifically taught that said instruction A causes the processor to retrieve a processor status from a stack. However, Hammer has taught that once the processor has finished processing an interrupt, normal processing is resumed, see column 1, lines 18-22, column 2, lines 35-39. Hammer has omitted the details of resuming normal processing after an interrupt. However, in order for the processor to resume normal processing after the interrupt is serviced, the processor status must be retrieved. Intel has taught interrupt instructions that cause the processor to retrieve a processor status from a stack for the desirable purpose of quickly

resuming execution of the interrupted instructions (Intel, page 4-16, lines 19-20 and page 4-16 lines 26-27. The contents of the EFLAGS, CS, and EIP registers are the processor status.). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have the instruction A of Hammer, cause the processor to retrieve a processor status from a stack, as taught by Intel, for the desirable purpose of quickly resuming execution of the interrupted instructions.

19. Referring to claim 6, Hammer and Intel have taught a method according to claim 5, as described above, and characterized in that instruction A causes the processor to store a return address on a stack (Intel, page 5-15 lines 20-23, A return address is stored on the stack by storing the CS and EIP registers).

20. Claims 8, 9, and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hammer et al., US Patent 5,901,309 (herein referred to as Hammer) in view of Miller et al., US Patent 6,081,884, cited by the Examiner in the action mailed on August 8, 2004 (herein referred to as Miller).

21. Referring to claim 8, Hammer has taught a system according to claim 7, as described above. Hammer has not taught that said instruction B is an element of an instruction bundle comprising a plurality of instructions; said pipeline comprising a plurality of execute stages for executing the plurality of instructions of said instruction bundle in a parallel fashion and said detection means precedes a plurality of execute stages. However, Miller has taught an instruction in an instruction bundle comprising a plurality of instructions (Miller, column 1, line 59-column 2, line 10, Figure 2); a pipeline comprising a plurality of execute stages for executing the plurality of instructions of said instruction bundle in a parallel fashion (Miller, column 1, line

59-column 2, line 10, Figure 2) for the desirable purpose of gaining performance by exploiting more parallelism (Miller, col. 2 lines 7-9) while utilizing a vast amount of existing code (Miller, col. 2 lines 30-35). Therefore it would have been obvious to one of ordinary skill in the at the time the invention was made to have instruction B, as taught by Hammer, be an element of an instruction bundle comprising a plurality of instructions and said pipeline comprising a plurality of execute stages for executing the plurality of instructions of said instruction bundle in a parallel fashion, as taught by Miller, for the desirable purpose of increasing performance by exploiting more parallelism (Miller, col. 2 lines 7-9) while utilizing a vast amount of existing code (Miller, col. 2 lines 30-35). Furthermore, when the concepts of Hammer are combined with Intel, as described above, the detection means will necessarily precede the plurality of execute stages.

22. Referring to claim 9, Hammer in combination with Miller have taught a system according to claim 8, as described above, and characterized in that said detection means is arranged to evaluate a bit pattern attached to said instruction bundle, said bit pattern marking the presence of said instruction type amongst said plurality of instructions (The opcodes of the instructions in the instruction bundle are attached and included in a VLIW instruction. Opcodes are evaluated and the presences of interrupt instructions are identified.).

23. Referring to claim 10, Hammer in combination with Miller have taught a system according to claim 8, as described above, and characterized in that said instruction bundle is a Very Long Instruction Word in a compressed form (Miller, column 1, line 59-column 2, line 10, Figure 2).

24. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hammer et al., US Patent 5,901,309 (herein referred to as Hammer) in view of Fowler et al., US Patent 5,455,918 (herein referred to as Fowler).

25. Referring to claim 11, Hammer has taught a system according to claim 7, as described above. Hammer has not specifically taught that the instruction A to be forced into a pipeline by said insertion means is present in the system in a hard-coded manner. However, Fowler has taught that implementing instructions in a hard-coded manner obviates the need for certain operations, such as instruction fetch from memory, thereby speeding up instruction execution (Fowler, column 2, lines 6-37). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have instruction A, as taught by Hammer, be present in the system in a hard-coded manner, as taught by Fowler, for the desirable purpose of speeding up instruction execution (Fowler, column 2, lines 6-37).

Response to Arguments

26. Applicant's arguments with respect to claims 1-12 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

27. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

28. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after

the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

29. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tonia L. Meonske whose telephone number is (571) 272-4170. The examiner can normally be reached on Monday-Friday, with every other Friday off.

30. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie P. Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

31. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

tlm

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100